applicant is intending to encompass." Applicant respectfully submits that the above statement is in error and mischaracterizes claims 107-122.

Claim 107 recites, *inter alia*, "[a] process for forming an interposer element for use as a chip carrier comprising the steps of: providing an insulating layer ... and processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, ... further comprising the step of forming at least one passive circuit device for use in radio frequency (RF) communications systems, said passive circuit device having at least one of said plurality of passive circuit elements."

Thus, the Office Action statement: "claims 107-122 provides a method for use in a various circuit devices" is incorrect. Instead, claim 107 recites, *inter alia*, "[a] process for forming an interposer element for use as a chip carrier."

Furthermore, the Office Action statement: "the claim does not set forth any steps involved in the method/process" is also incorrect. Claim 107 recites, *inter alia*, the positive step of "forming at least one passive circuit device for use in radio frequency (RF) communications systems, said passive circuit device having at least one of said plurality of passive circuit elements." As noted, claim 107 also recites, *inter alia*, the steps of "providing an insulating layer ... and processing said insulating layer to produce at least one passive circuit element on or within said insulating layer."

Moreover, Applicants respectfully submit that the cases cited in the Office Action, Ex parte Dunki, 153 U.S.P.Q. 678 (Pat. Bd. App. 1967) and Clinical Products Ltd. v. Brenner, 255 F. Supp. 131 (D.D.C. 1966), are inapposite. Both of these cases involved claims directed to a "use" without reference to any process or method. In Dunki, the disputed claim recited, "12. The use of a high carbon austenitic iron alloy having a proportion of free carbon as a vehicle brake part subject to stress by sliding friction." Dunki, 153 U.S.P.Q. at 678. In Clinical Products, the claim at issue recited, "41. The use as a sustained release therapeutic agent in the body of ephedrine adsorbed upon polystyrene sulphonic acid." Clinical Products, 255 F. Supp. at 132. In contrast to the presently

pending claims 107-122, neither of the claims cited in Dunki or Clinical Products include any language referring to a method or process, nor do they include any steps for performing a claimed method or process. As noted, claim 107 recites a specific process, as well as positive steps of the process.

The rejection of claims 108-122 under 35 U.S.C. § 112 should be withdrawn for similar reasons.

Claim 122 stands further rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action states, "[i]t is not clear how an active circuit element is formed on the insulating layer if Applicant forms the passive circuit element on the same insulating layer while bonding an integrated circuit chip to the interposer layer." Applicants respectfully submit that this statement in the Office Action mischaracterizes the present invention.

Claim 122 recites, *inter alia*, "providing an insulating layer to both surfaces of said silicon substrate [and] processing said insulating layer to produce at least one active circuit element." Thus, the statement in the Office Action: "[i]t is not clear how an active circuit element is formed on the insulating layer" is in error. Claim 122 clearly recites "processing said insulating layer to produce at least one active circuit element." The claim need not define how this is done to be definite. All that is required is that one skilled in the art be able to know the metes and bounds of the claimed invention. The claims do this. A technique for processing the insulating layer to produce an active circuit element is described in the specification: "[a]lternatively, the interposer substrate 100 may also have active devices built on or into the insulating layers 104 on one or both sides of the substrate 100." Specification at page 19, lines 11-13. Processing techniques to provide active circuit elements in a layer are well known in the art of semiconductor manufacturing.

Furthermore, neither the specification nor the claims of the present application refer to an "interposer layer." Claim 122 recites, inter alia, a "process for forming an

interposer element ... comprising the step of bonding at least one integrated circuit chip to the interposer element." No "interposer layer" is recited. Applicants respectfully request that this ground of rejection be withdrawn.

Claims 88-100, 105-118 and 123 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,770,476 to Stone ("Stone") in view of U.S. Patent No. 6,201,287 B1 to Forbes ("Forbes"). Reconsideration is respectfully requested.

Claim 88 recites, *inter alia*, "[a] process for forming an interposer element for use as a chip carrier comprising the steps of: providing an insulating layer on at least one surface of a silicon substrate; and processing said insulating layer to produce at least one passive circuit element on or within said insulating layer." According to claim 88, the "passive circuit element [is] separated from said silicon substrate by a portion of said insulating layer ... having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate."

Stone is directed to an interposer having at least one passive electronic structure positioned within the interposer structure. As noted in the Office Action, Stone fails to disclose an interposer having an insulating layer on at least one surface of a silicon substrate. Also as noted in the Office Action, Stone fails to disclose at least one passive circuit element being separated from the silicon substrate by a portion of the insulating layer. Additionally, the Office Action states that Stone fails to disclose that the separating portion of the insulating layer has a thickness such that the at least one passive circuit element is electrically shielded from the silicon substrate. Claims 89-123 depend from claim 88 and hence each includes these features not disclosed or suggested by Stone.

Forbes relates to monolithic inductance-enhancing integrated circuits, inductor assemblies, and inductance-multiplying methods, including in FIG. 9 first and second inductors 32, 34 received within an insulative material layer 36. Forbes fails to disclose or suggest any interposer structure whatsoever, nor any "passive circuit element being separated from said silicon substrate by a portion of said insulating layer ... having a

thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate."

The Office Action states, "Forbes in the U.S. patent 6,201,287 B1; figures 1-10 and related text, shows forming a passive circuit element 32 in an insulating layer 36 that is on at least one surface of a silicon substrate 100 ..." Even if Forbes discloses an insulating layer 36 on at least one surface of a silicon substrate 100, Forbes fails to disclose or suggest an "insulating layer ... having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate." Forbes does not mention a thickness for "insulative material layer 36" and certainly does not disclose or suggest that the layer 36 have a thickness "such that said at least one passive circuit element is electrically shielded from said silicon substrate."

Because the Office Action notes that Stone fails to disclose or suggest features of claims 88-123, and because Forbes fails to disclose or suggest these features, this rejection should be withdrawn. Stone and Forbes, whether taken singly or in combination, fail to disclose or suggest the features of claims 88-123.

Claims 101-104 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stone and Forbes, and further in view of U.S. Patent No. 5,912,044 to Farooq et al. ("Farooq"). Reconsideration is respectfully requested.

Farooq discloses a method for forming thin film capacitors by a multi-level dry processing technique. Farooq fails to disclose or suggest "at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer ... having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate." As noted, claims 101-104 depend from claim 88 and hence include features not disclosed or suggested by Farooq, Stone and Forbes, whether taken separately or in combination.

Claims 119-121 stand rejected under 35 U.S.C. § 103 as being unpatentable

over Stone and Forbes, and further in view of U.S. Patent No. 6,121,676 to Solberg ("Solberg"). Reconsideration is respectfully requested.

Solberg discloses a method of making a stacked microelectronic assembly. In the Solberg assembly, semiconductor chips may be stacked vertically one atop the other, for example a plurality of stacked semiconductor chip assemblies is disclosed wherein each assembly includes an interposer and a semiconductor chip mounted thereto. Solberg specification, col. 1, lines 6-67, and col. 2, lines 1-8. Solberg fails to disclose or suggest "at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer ... having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate." Claims 119-121 depend from claim 88 and hence include these features.

Thus, the features of claims 119-121 are not disclosed or suggested by Stone, Forbes and Solberg, whether taken separately or in combination, and thus this rejection should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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